3U VPX AMD VERSAL™ Prime or AI Edge Gen2 with FMC Site

Overview

PanaTeQ's VPX3-VERSA1 is a 3U OpenVPX module based on AMD Versal™ Prime Series Gen 2 or AMD Versal™ AI Edge Series Gen 2 adaptive SoCs.

The VERSAL™ integrates up to 8-core ARM Cortex-A78A based Application Processing Unit (APU), up to 10-core ARM Cortex-R52 based Real-Time Processing Unit (RPU), DSP Engines, AI Engines (AI Edge devices only) and a large Programmable Logic (PL) in a single device. It also includes on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces.

The board can be ordered with different versions of the VERSAL™ family of devices, coupled up to 40GB 32-bit LP-DDR5 Memory with ECC.

256GB of soldered eMMC managed NAND Flash is available for local data storage.

The VPX3-VERSA1 uses advanced DC/DC power modules from Analog Devices using PMBus and PanaTeQ's Smart Power Management technology.

For front-end I/O interfaces, an on-board FMC site compliant to the VITA 57.1 HPC standard with 68 SE IO (34 Diff Pairs) and 10 MGTs, allowing a wide range of applications such as electronic warfare (EW) systems , High-Speed Communication, LIDAR/RADAR/SONAR.

The board can act as a Single Board Computer in the VPX system. When the VPX3-VERSA1 is System Controller, there is no need to add any SBC in the VPX System, improving Size, Weight, Power and Cost (SWaP-C).

A large number of the peripherals are available on the VPX backplane: 1x ETH 1000Base-T, 1x USB 2.0, 4x RS-232 or 2x Full-Duplex RS-422, 16x GPIOs, 1x CAN-FD.

The air cooled PanaTeQ System Development Kit **VPX3-VERSA1-PSDK** is available for the developers and includes a lab chassis with 3-slots Centralized backplane, the VPX3-VERSA1-A1N-AS and RTM-VERSA1 boards, a PetaLinux BSP, PanaTeQ FPGA Design References and cables.

Key Features

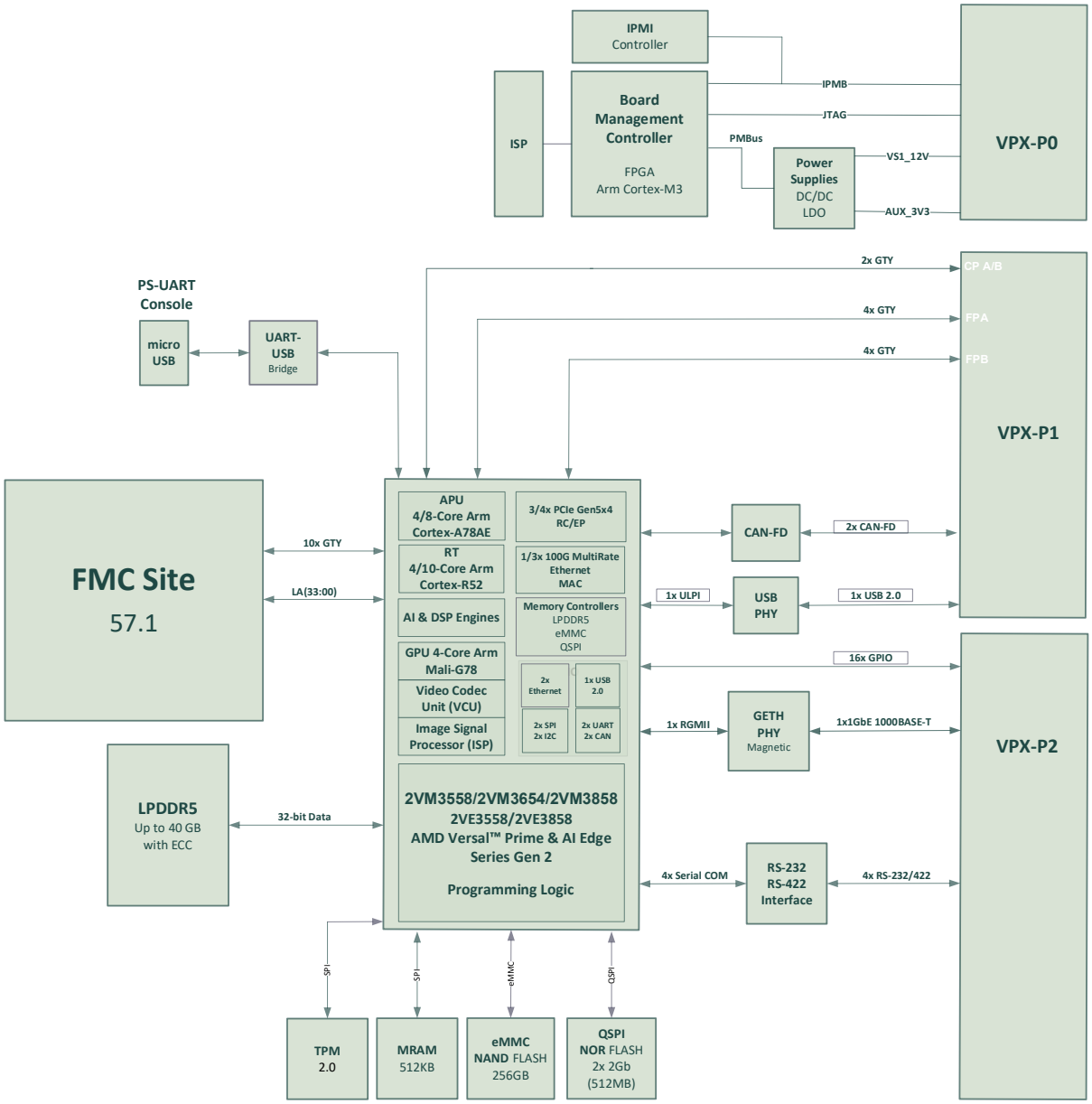
- 3U VITA 46.0, 46.4, 46.6, 65.0 Compliant.
- Optional **SOSA Aligned** version **VPX3-VERSA1S.**
- **AMD Versal™™ Prime & AI Edge Gen2 Series** SSVA2112 Package.
- **Versal™ Prime Gen2: 2VM3558/2VM3654/2VM3858.**
- **Versal™ AI Edge Gen2: 2VE3558/2VE3858.**
- Up to 8 Arm Cortex-A78AE cores.
- Up to 10 Arm Cortex-R52 cores.
- DSP Engines up to 2064. AI Engines up to 144 (AI Edge only).
- 20GB or 40GB LPDDR5 with ECC.
- 512MB (2x 2Gb) QSPI NOR, eMMC 256GB, MRAM 512KB.
- Flash-memory-based trusted platform module (TPM 2.0) connected to PS-SPI.
- 8x MGTY on VPX-P1, PCIe Up to Gen5 support.
- 2x ETH 1000Base-X/SGMII on VPX-P1 Control Plane.
- 16x GPIOs on VPX-P2
- 1x ETH 1000Base-T on VPX-P2
- 4x RS232 or 2x Full-Duplex RS422 on VPX-P2
- 1x USB 2.0 on VPX-P1.
- DiplayPort Video Output on VPX-P1.
- FMC site compliant with VITA 57.1 HPC, with 68 single-ended I/Os or 34 differential pairs and 10 MGTs.
- Smart Power Management using DC/DC with PMBus.
- Board Management Controller ARM Cortex-M3 based.
- VPX System and IPMI controllers.
- Air Cooled and Conduction Cooled.
- Optional KVPX connectors.

Typical Applications

- Rugged real-time video processing systems
- AI-based object detection and tracking
- UAV, airborne and autonomous platform vision
- Defense, surveillance and ISR payloads
- Multi-camera sensor fusion systems
- Mission computer video acceleration
- Low-latency video compression and streaming
- Industrial machine vision and inspection

VITA Open Standards, Open Markets — OpenVPX™

Block Diagram



AMD Versal™ Prime & AI Edge Series Gen 2
Overview

VERSAL™ Prime & AI Edge Series Gen2 Block Diagram

Processing System
Up to 8x Arm® Cortex®-A78AE application processors and up to 10x Cortex-R52 real-time processors designed to offer over 200k DMIPs of total compute with support for USB 3.2, DisplayPort™ 1.4, 10 GbE, PCIe® Gen5, and additional peripherals.

Programmable Logic & I/O
World-class Versal™ programmable logic and new high-performance X5IO with MIPI C-PHY support provide flexibility, real-time processing, and future adaptability.

AI Engines
New AIE-ML v2 tiles designed to deliver 2X compute/tile compared to previous generation, robust energy efficiency, and new native data types—including MX6 & MX9 designed to boost throughput & performance/watt.

Safety and Security Features
Upgraded safety and security features include ASIL D / SIL 3 operation of the processing system, NoC, memory controllers, a new application security unit, and other security enhancements over the previous generation.
The processing system offers up to 100k DMIPs of compute for ASIL D / SIL 3 applications.

Hard Image/Video Processing
New hard image signal processor (ISP) IP accelerates image processing and enhanced video codec unit (VCU) tiles support HEVC & AVC 4K60 4:4:4, 12-bit encode & decode.

DDR5 & LPDDR5X
Hard DDR memory controllers support DDR5-6400 and LPDDR5X 8533 with new inline crypto functionality—offering up to 170 GB/s memory bandwidth.

Integrated GPU
An Arm Mali™-G78AE GPU enables display/HMI applications at up to 4K60 resolutions with up to 268 GFLOPs of compute.
Read the white paper for additional information.

Board Specifications

3U VPX Interfaces

- VITA 46.0/46.4/46.6/65.0 VPX/OpenVPX Specifications compliant.
- Optional SOSA Aligned VPX3-VERSA1S. Please contact us for more details.
- Up to 8x MGTY connected to/from VERSAL™ device. PCIe x4 up to Gen5 support.
- 2x 1000BASE-X/SGMII links on VPX Control Plane.
- 1x 1000BASE-T, 4x RS-232 or 2x Full-Duplex RS-422, 1x USB 2.0, 16x GPIOs, 1x CAN-FD.
- On-board IPMI SOSA compliant, System Controller. JTAG Support.

OpenVPX VITA 65.0 Profiles

- MOD3-PAY-1F2F2U-16.2.2-n using slot profile **SLT3-PAY-1F2F2U-14.2.2**

SOSA Aligned Profiles

- Optional SOSA-aligned VPX3-VERSA1S variant under definition. Please contact PanaTeQ for details.

AMD Versal™™ Prime and AI Edge Series Gen 2

- Supported Prime Gen2 Devices:2VM3558/2VM3654/2VM3858 SSVA2112 Package (Speed Grade –1/2/3).
- Supported AI Edge Gen2 Devices:**2VE3558/2VE3858 SSVA2112** Package (Speed Grade –1/2/3).
- Processing System : Up to 8 Cores Arm® Cortex®-A78AE, 64 KB I w/parity & D w/ECC L1 Cache, 512 KB L2 Cache.
- Real-Time Processing Unit : Up to 10 Arm Cortex-R52, 32 KB L1 Cache w/ECC, 128 KB TCM w/ECC.
- Programmable Logic: 492,188 Logic Cells (**2VM3558/2VE3558**) /1,188,040 Logic Cells (**2VM3858/2VE3858**).
  225,000 LUTs (**2VM3558/2VE3558**) / 543,104 LUTs (**2VM3858/2VE3858**).
- On-Chip Memories: 23.9Mb (**2VM3558/2VE3558**) / 97.0Mb (**2VM3858/2VE3858**).
- AI Engines: 96 (**2VE3558**) / 144 (**2VE3858**).
- DSP Engines: 700 (**2VM3558/2VE3558**) / 2064 (**2VM3858/2VE3858**).
- Hard IPs: 3x PCIe Gen5x4, 3x 100G Multirate Ethernet MAC.
- High Speed Serial Links: 12/20 full duplex, high performance, GTY Multi-Gigabit Transceivers (MGT) @ up to 32.75 Gb/s.

External Memories

- Up to 40GB of LPDDR5 Programmable Logic (PL) memory, 32-bit data, with ECC.
- 256GB eMMC of managed NAND Flash memory. HS200 support @ up to 100MB/s.
- 512KB of SPI MRAM (NVRAM), Flash-memory-based trusted platform module (TPM 2.0).
- 2x 2Gb (512MB) of QSPI NOR Flash memory for booting VERSAL™ Programmable Logic and Firmware Processing System.

FMC Slot

- Compliant to the VITA 57.1 specification.
- 10x high-performance MGTs to/from VERSAL™ Programmable Logic.
- 68x SE or 34x DIFF LA[33:0] to/from VERSAL™ Programmable Logic.
- 2x clocks FMC to VERSAL™ Programmable Logic.
- 2x clocks FMC to VERSAL™ MGT, 2x bidirectional clocks.
- VADJ = 1V8.

Board Management Controller (BMC)

- Based on Microchip SmartFusion Customizable System-on-Chip (**cSoC**) with on-chip Arm Cortex-M3 at up to 100MHz.
- Real-Time Monitoring+Alarms: Voltages, Currents, Temperatures, 6-Axis Accelerometer, Magnetometer and Humidity.
- Reset Management, Power-Up and Power-Down Sequencing. Built-In Test (**BIT**).
- Large private 32MB Event Log Flash Memory.
- UART communication with host using RTM-VERSA1 Rear-Transition Module.
- Smart Power Management using Analog Devices DC/DC modules with Digital Power System Management.
- On-board VPX System and IPMI controllers.

Environmental Specifications

- Compliant with VITA 47 specification. Please contact PanaTeQ for more information.

Product Codification

The VPX3-VERSA1 can be assembled with different versions of the VERSAL™ devices and various amounts of memory storage.
Full MGT population depends on the selected Versal™ Gen2 device.
Devices with 12 MGTs support a reduced high-speed I/O configuration. Full VPX + FMC MGT capability requires a 20-MGT device option.
Supported device options, subject to AMD availability and lifecycle status.
The cooling technique and ruggedization level are also available options.
The following table shows the product coding for all these options.

VPX3-VERSA1– abc–rl–e–k

a	Device	APU Arm A78AE	RT Arm Cortex-R52	AI AIE-ML v2 Tiles	DSP Engines	Arm Mali-G78AE GPU	Video Codec Unit (VCU)	Image Signal Processor (ISP)	MGTs	Logic Cells	LUTs	PL Memory
A	2VM3558	8-Core	10-Core	0	700	4-Core	1	0	12	492,188	225,000	23.9 Mb
B	2VM3654	4-Core	6-Core	0	1428	1-Core	2	0	20	695,800	318,080	55.2 Mb
C	2VM3858	8-Core	10-Core	0	2064	4-Core	1	0	20	1,188,040	543,104	97.0 Mb
D	2VE3558	8-Core	10-Core	96	700	4-Core	1	3	12	492,188	225,000	23.9 Mb
E	2VE3858	8-Core	10-Core	144	2064	4-Core	1	3	20	1,188,040	543,104	97.0 Mb

b	Device Speed Grade
1	Slowest
2	Mid
3	Highest

c	LPDDR5 Memory
N	20GB
M	40GB

rl	Ruggedization Level	VITA 47
AS	Air Standard	EAC4
AR	Air Rugged	EAC6
CC	Conduction Cooled	ECC3

e	Tropicalization
E	Conformal Coating

k	Backplane Connectors
K	KVPX Connectors

Ordering Information

The following product references are offered by PanaTeQ as standard products.

Other combinations of devices, speed grade, memory and cooling can be specially ordered. Please contact us for details

Reference	Description
RTM-VERSA1	Rear Transition Module for VPX3-VERSA1
VPX3-VERSA1-PSDK-A-A1N-AS	VPX3-VERSA1-A1N-AS System Development Kit

Reference	Device	Speed Grade	Memory LPDDR5	Ruggedization Level
VPX3-VERSA1-A1N-AS	2VM3558	-1	20GB	Standard Air Cooled

PanaTeQ Contact

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Available from: