

## 3U VPX AMD VERSAL Prime + AD9084 Module

### Overview

PanaTeQ's VPX3-VERSA2-MxFE4 is a 3U VPX OpenVPX/SOSA module based on the **VERSAL Prime** Adaptive SoC device from AMD and one **AD9084** Apollo MxFE device from Analog Devices for a broad range of applications such as Software Defined Radio, MILCOM, massive MIMO, Phase Array Radar and Electronic Warfare.

The **AD9084** mixed signal front-end (MxFE®) is a highly integrated device with a 16-bit, 28 GSPS maximum sample rate, RF digital-to-analog converter (DAC) core, and 12-bit, 20 GSPS maximum sample rate, RF analog-to-digital converter (ADC) core. The AD9084 supports four transmit channels and four receive channels.

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These devices features a 48 lane, 32.5 Gbps JESD204C or 20 Gbps JESD204B data transceiver port, an on-chip clock multiplier, and a digital signal processing (DSP) capability targeted at either wideband or multiband, direct to RF applications.

The AD9084 also features a bypass mode that allows the full bandwidth capability of the ADC and/or DAC cores to bypass the DSP datapaths

The **VERSAL Prime** integrates a Dual-core ARM Cortex-A72 based Application Processing Unit (**APU**), a Dual-core ARM Cortex-R5F based Real-Time Processing Unit (**RPU**), DSP Engines and a large Programmable Logic (**PL**) in a single device. It also includes on-chip memory, external memory interfaces, and a rich set of peripheral connectivity interfaces.

The board can be ordered with different versions of the VERSAL family of devices, coupled up to 4 or 8GB 64-bit DDR4-3200 Processing Memory with 8-bit ECC.

2GB 32-bit of LPDDR4-2133 is also available as the Programmable Logic Memory, allowing data streaming applications such as video CODEC and signal processing. 256GB of soldered eMMC managed NAND Flash is available for local data storage.

The VPX3-VERSA2 uses advanced DC/DC power modules from Linear Technology using PMBus and PanaTeQ's **Smart Power Management** technology.

The board can act as a **Single Board Computer** in the VPX system. When the VPX3-VERSA2 is System Controller, there is no need to add any SBC in the VPX System, improving **Size, Weight, Power and Cost** (SWaP-C).

A large number of the peripherals are available on the VPX backplane: 1x ETH 1000Base-T, 1x USB 2.0, 4x RS-232 or 2x Full-Duplex RS-422, 16x GPIOs, 2x CAN-FD.

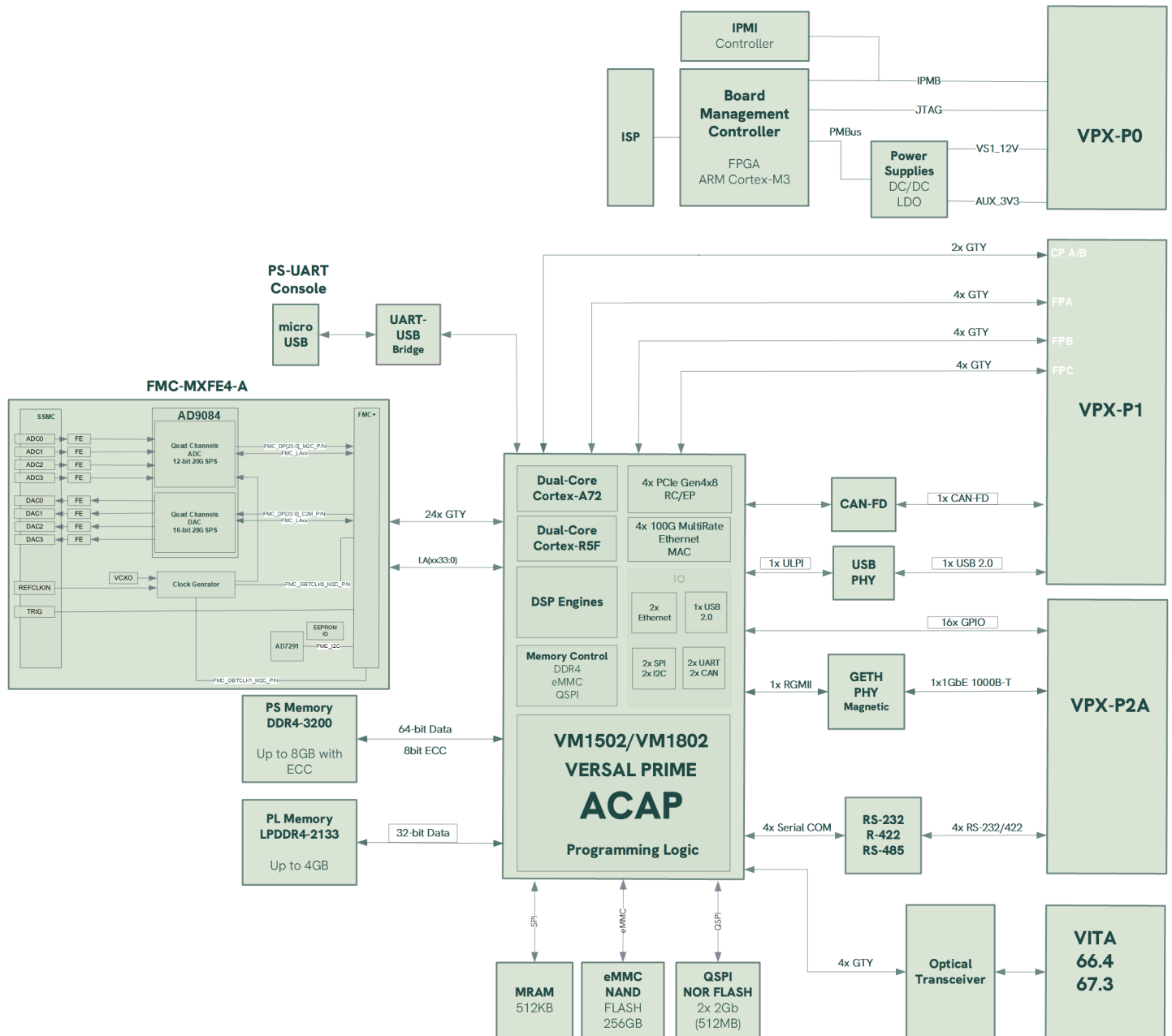
### Key Features

- 3U VITA 46.0, 46.4, 46.6, 65.0 Compliant
- Optional **SOSA Aligned** version **VPX3-VERSA2S-MxFE4**
- 4T4R **AD9084** Apollo MxFE Quad, 16-Bit, 28 GSPS RF DAC and Quad, 12-Bit, 20 GSPS RF ADC
- AMD VERSAL Prime Series based
- VM1502/1802 VSVC1760 Package
- Dual Core Arm A72 up to 1.7 GHz
- Dual Core Arm R5F up to 750 MHz
- DSP Engines up to 1968
- 4 or 8GB DDR4-3200 64-bit PS memory with 8-bit ECC
- 2GB LPDDR4-2133 32-bit PL memory
- 512MB (2x 2Gb) QSPI NOR, eMMC 256GB, MRAM 512KB
- 12x MGTy on VPX-P1, PCIe Up to Gen4 support
- 2x ETH 1000Base-X/SGMII on VPX-P1 Control Plane
- 18x GPIOs on VPX-P2
- 1x ETH 1000Base-T on VPX-P2
- 4x RS232 or 2x Full-Duplex RS422 on VPX-P2
- 1x USB 2.0 on VPX-P1
- FMC+ VITA 57.4 site with 68x IOs, up to 24x MGTs.
- Optional 4x Full-Duplex Optical Links VITA 66.4
- Optional 10x NanoRF VITA 67.3
- Smart Power Management using DC/DC with PMBus
- Board Management Controller ARM Cortex-M3 based
- VPX System and IPMI controllers
- Air Cooled and Conduction Cooled
- KVPX Connectors in option

### Typical Applications

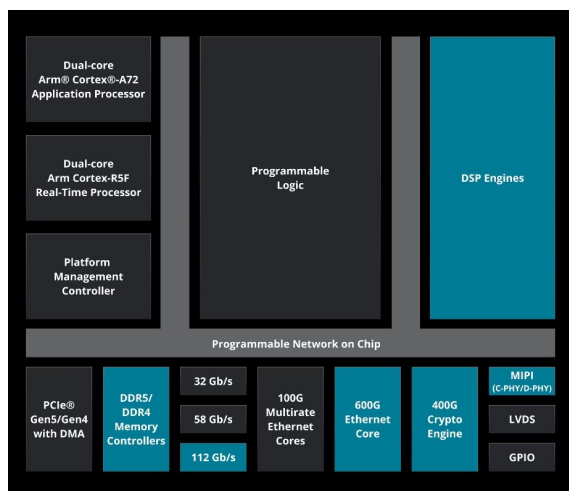
- MILCOM
- Software Defined Radio
- MIMO
- Electronic Warfare
- Signal Intelligence
- Radar

## Block Diagram



## AMD VERSAL Prime Adaptative Compute Acceleration Platform (ACAP)

### VERSAL Prime Series Block Diagram



### Architecture

Versal ACAPs are built around an integrated shell composed of a programmable network on chip (NoC), which enables seamless memory-mapped access to the full height and width of the device. ACAPs comprise: a multicore scalar processing system (PS); an integrated block for PCIe® with DMA and Cache Coherent Interconnect Designs (CCP); SIMD VLIW AI Engine accelerators for artificial intelligence and complex signal processing; and Adaptable Engines in the programmable logic (PL). Together, these form a platform for fast time-to-market (TTM) compute acceleration for cloud, edge, and networking applications. The platform management controller (PMC), adjacent to the PS, is responsible for booting and configuring the device. Versal devices typically have I/O and memory controllers on the north and south edges of the device and serial transceivers on the east and west edges. The NoC spans full height and width of the device.

### Compute and Acceleration

Every Versal ACAP has Scalar Engines that comprise a dual-core Arm® Cortex®-A72 (APU) and a dual-core Arm Cortex-R5F (RPU) in the PS. The PS includes a number of peripherals for communication standards, including gigabit Ethernet and USB 2.0, and controllers for SPI, I2C, UART, and CAN-FD. The PS accesses the DDR memory controllers on the top and bottom of the device through the NoC. In addition to interfacing to external memory, the APU includes: Level 2 (L2) cache; the RPU includes tightly coupled memory (TCM); and both APU and RPU have access to the on-chip memory (OCM). The PL is made up of configurable logic blocks, containing 6-input look-up tables (LUTs) and flip-flops; different-sized memory blocks; 36Kb block RAM and 288Kb UltraRAM; digital signal processing (DSP) blocks; and a wealth of interconnect, switches, and muxes to connect blocks together. All resources are arranged in columns. The PL is divided into regions that are a fixed height. Each region has its own clocking capabilities and NoC access points.

### Platform Management

The PMC resides adjacent to, but is independent from, the PS. It is responsible for the boot and configuration of the device from the primary boot source. The PMC is also responsible for configuring the PL, which can be configured before or after the PS. It also controls encryption, authentication, system monitoring, and device debug capabilities of the platform.

### Connectivity

The south edge of the Versal ACAPs typically contains a number of XPIO banks and associated memory controllers to read from and write to DDR4 and LPDDR4 memory. XPIO can be used independently from the dedicated memory controllers for many functions, including any with soft memory controllers created in the PL. The east and west edges of the device typically contain serial transceivers capable of communicating up to 112Gb/s. The PL can also contain integrated blocks for high-value functions, such as the integrated block for PCIe (PL PCIE) with support for Compute Express Link (CXL), multirate Ethernet MAC, 600G Ethernet MAC, 600G Interlaken, and 400G High-Speed Crypto (HSC) Engine.

## Board Specifications

### 3U VPX Interfaces

- VITA 46.0/46.4/46.6/65.0 VPX/OpenVPX Specifications compliant
- Optional SOSA Aligned VPX3-VERSA2S. Please contact us for more details
- 12x MGTY connected to/from VERSAL device. PCIe x8 Gen4 support
- 2x 1000BASE-X/SGMII links on VPX Control Plane
- 1x 1000BASE-T, 4x RS-232 or 2x Full-Duplex RS-422, 1x USB 2.0, 16x GPIOs, 2x CAN-FD.
- Optional 4x Full-Duplex Optical Links VITA 66.4 or 66.5. Please contact us for more details
- Board Management Controller (BMC) Interface. VITA 46.11 Ready
- System Controller capability
- JTAG

### OpenVPX VITA 65.0 Profiles

- MOD3-PAY-8U-16.2.9-1, MOD3-PAY-8U-16.2.9-2
- Optional 4x Full-Duplex Optical Links VITA 66.4 or 66.5. Please contact us for more details

### SOSA Aligned Profiles

- Please contact us for more details

### AMD VERSAL Prime

- Supported Devices: **VM1502** / **VM1802** VSVC1760 Package (Speed Grade -1/2)
- Processing System : Dual-Core ARM A72, Dual-Core ARM R5F, 2x USB, 2x GETH MACs
- Programmable Logic: 981K Logic Cells (VM1502) / 1968K Logic Cells (VM1802)  
448612 LUTs (VM1502) / 899840 K LUTs (VM1802)
- On-Chip Memories: 178Mb (VM1502) / 191Mb (VM1802)
- DSP Engines: 1312 (VM1502) / 1968 (VM1802)
- Hard IPs: 4x PCIe Gen4x8, 4x 100G Multirate Ethernet MAC
- High Speed Serial Links: 44 full duplex, high performance, GTY Multi-Gigabit Transceivers (MGT) @ up to 32.75 Gb/s
- Supported by PanaTeQ's FPGA Development Kit

### External Memories

- Up to 8GB of DDR4-3200 Processor System (PS) memory, 64-bit data, 8-bit ECC
- Up to 4GB of LPDDR4-2133 Programmable Logic (PL) memory, 32-bit data, no ECC
- 256GB eMMC of managed NAND Flash memory. HS200 support @ up to 100MB/s
- 512KB of SPI MRAM (NVRAM)
- 2x 2Gb (512MB) of QSPI NOR Flash memory for booting VERSAL Programmable Logic and Firmware Processing System

### Analog Devices Apollo MxFE

- AD9084  
4x 12-bit ADC @ up to 14 GSPS  
4x 16-bit DAC @ up to 28 GSPS

### Board Management Controller (BMC)

- Based on Microsemi SmartFusion Customizable System-on-Chip (**cSoC**) with on-chip ARM Cortex-M3 at up to 100MHz
- Real-Time Monitoring+Alarms: Voltages, Currents, Temperatures, 6-Axis Accelerometer, Magnetometer and Humidity
- Reset Management, Power-Up and Power-Down Sequencing. Built-In Test (**BIT**)
- Watchdogs (Avionics type)
- Large private 32MB Event Log Flash Memory.
- UART communication with host using RTM-VERSA1 Rear-Transition Module
- Smart Power Management using Linear Technology DC/DC modules with Digital Power System Management.
- On-board VPX System and IPMI controllers.

## Product Codification

The **VPX3-VERSA2-MxFE4** can be assembled with different versions and various amounts of memory storage. The cooling technique et ruggedization level are also available options. The following table shows the product coding for all these options.

## VPX3-VERSA2-MxFE4 – a b c – rl

a	VERSAL Device	DSP Engines	Logic Cells	LUTs	Memory
A	VM1502	1312	981K	448512	178 Mb
B	VM1802	1968	1968K	899840	191 Mb

b	Device Speed Grade
1	Standard
2	Fast

c	PS / PL Memory Size
N	4GB/2GB
M	8GB/4GB

	Ruggedization Level	VITA 47
AS	Air Standard	EAC4
AR	Air Rugged	EAC6
CC	Conduction Cooled	ECC3

## Ordering Information

The following product references are offered by Panateq as standard products. Other combinations of devices, speed grade, memory and cooling can be specially ordered. Please contact us for details

Reference	VERSAL	MxFE	RF IO	Memory PS/PL	Ruggedization Level
<b>VPX3-VERSA2-MxFE4-A1N-AS</b>	VM1502	AD9084	4T4R	4GB/2GB	Air Standard

Reference	Description
<b>RTM-MxFE4-A</b>	Rear Transition Module for VPX3-VERSA2-MxFE-A
<b>VPX3-VERSA2-MxFE4-A1N-AS-PSDK</b>	VPX3-VERSA2-MxFE4-A1N-AS PanaTeQ System Development Kit

PanaTeQ Contact

Available from:

info@panateq.com