FMC Wideband RF Transceiver ADRV9026 based

Overview

The FMC-ZU3RF-A is a FMC for RF wireless communications applications based on the ADRV9026 component from Analog Device Inc (ADI). The ADRV9026 is a highly integrated, radio frequency (RF) agile transceiver offering four independently controlled transmitters, dedicated observation receiver inputs for monitoring each transmitter channel, four independently controlled receivers, integrated synthesizers, and digital signal processing functions providing a complete transceiver solution.

The device provides the performance demanded by cellular infrastructure applications, such as small cell base station radios, macro 3G/4G/5G systems, and massive multiple in/multiple out (MIMO) base stations.

The receiver subsystem consists of four independent, wide bandwidth, direct conversion receivers with wide dynamic range.

The four independent transmitters use a direct conversion modulator resulting in low noise operation with low power consumption. The device also includes two wide bandwidth, time shared, observation path receivers with two inputs each for monitoring transmitter outputs. The complete transceiver subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, eliminating the need for these functions in the digital baseband.

Other auxiliary functions such as analog-to-digital converters (ADCs), digital- to-analog converters (DACs), and general-purpose input/ outputs (GPIOs) that provide an array of digital control options are also integrated. To achieve a high level of RF performance, the transceiver includes five fully integrated phase-locked loops (PLLs). Two PLLs provide low noise and low power fractional-N RF synthesis for the transmitter and receiver signal paths.

A third fully integrated PLL supports an independent local oscillator (LO) mode for the observation receiver. The fourth PLL generates the clocks needed for the converters and digital circuits, and a fifth PLL provides the clock for the serial data interface. A multichip synchronization mechanism synchronizes the phase of all LOs and baseband clocks between multiple ADRV9026 chips.

All voltage controlled oscillators (VCOs) and loop filter components are integrated and adjustable through the digital control interface.

PanaTeQ offers the VPX3-ZU1B-SDR-DB development system based on the VPX3-ZU1B 3U OpenVPX Zynq Ultrascale+ and the FMC-ZU3RF-B-W1A-AS for typical Software Defined Radio application, in both air-cooled and conduction cooled version.

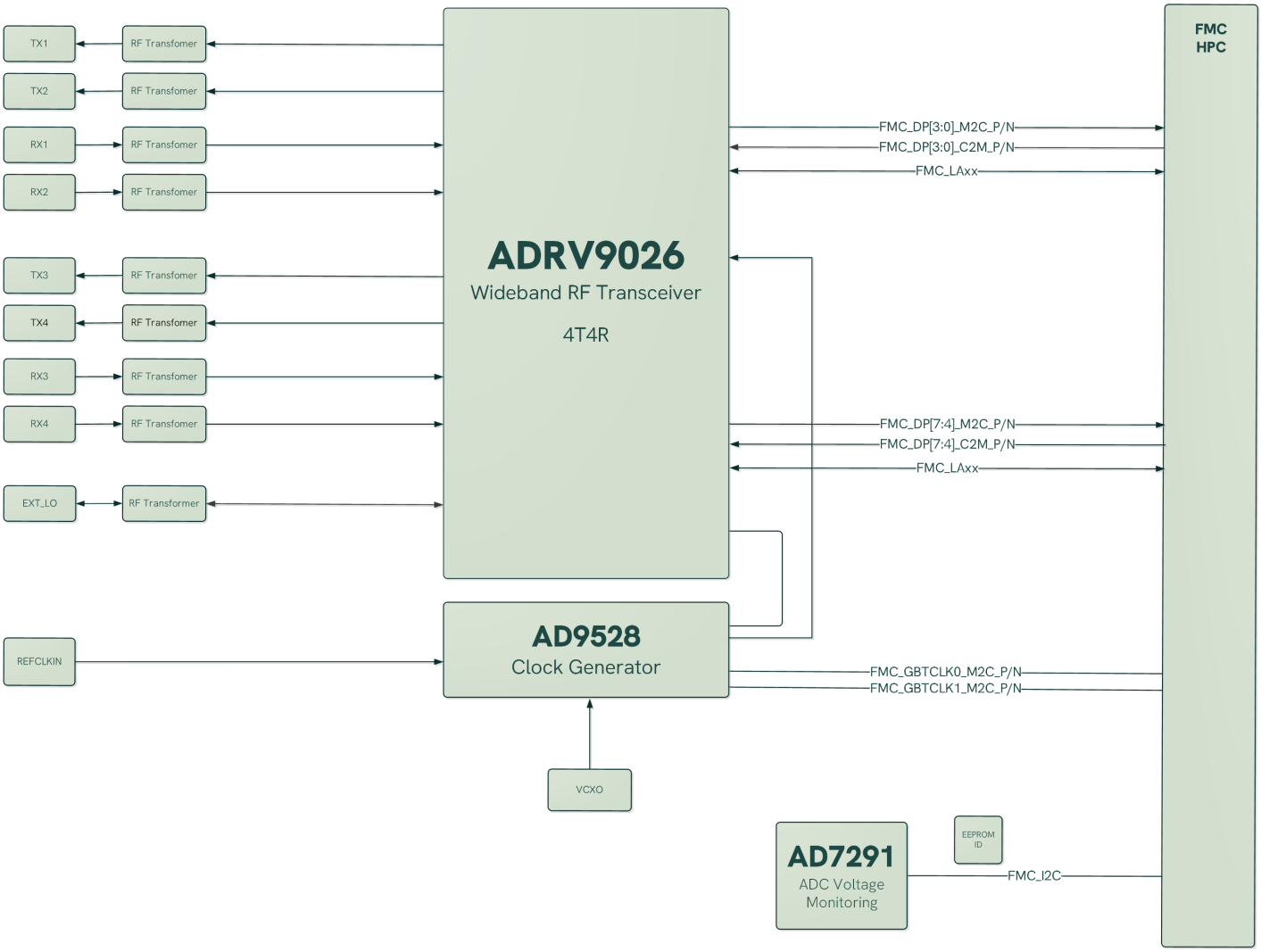
Key Features

- VITA 57.1-2010 specification compliant
- Fully HW/SW compatible with ADRV9026 Evaluation Board
- FMC High Pin Connector (HPC)
- JESD024B/C interface up to 24.33 Gbps
- - 4x Tx
- - 4x Rx
- LA Bus LVDS and Singled-Ended
- Operates with VAdj = 2.5V to 1.5V
- Air and Conduction Cooled compatible design
- 4x SSMC for Dual Transmitters (Tx)
- 4x SSMC for Dual Receivers (Rx)
- 1x SSMC Ext_Lo Input/Output
- 1x SSMC External Reference Clock Input
- RF Coverage: 75MHz to 6.0 GHz
- Tx Synthesis Bandwidth Max: 450MHz
- Rx Bandwidth Max: 200MHz
- Support Time Division Duplex (TDD)
- Support Frequency Division Duplex (FDD)
- Fully integrated independent fractional-N radio frequency synthesizers
- On-board VCXO : 100.000MHz, 122.880MHz, 125.000MHz, 153.600MHz or 156.250MHz

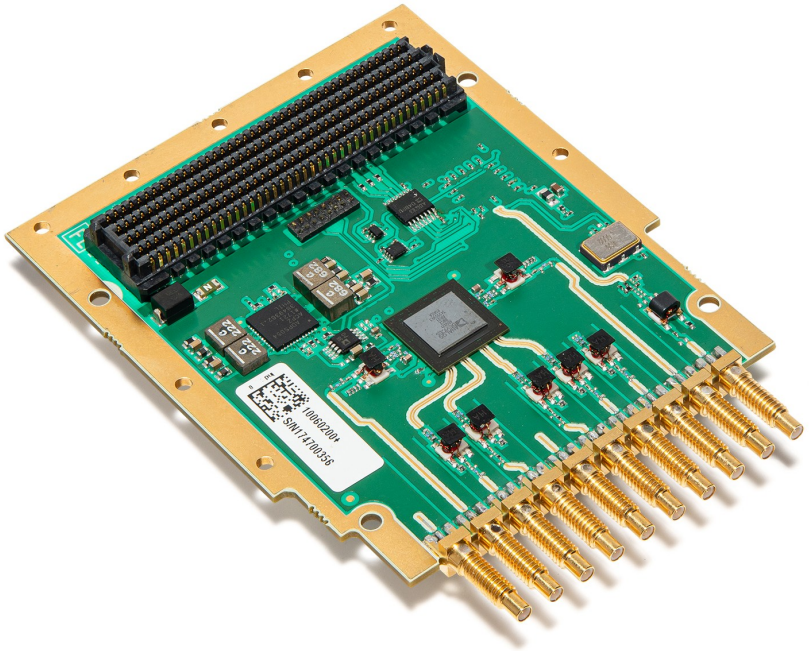
Typical Applications

- Software Defined Radio, Military Communications
- Wireless Infrastructure 3G/4G/5G
- TDD and FDD active Antenna Systems
- Electronic Warfare
- Drones and UAVs
- Phase Array RADAR

Bloc Diagram



Board Picture



Board Specifications

FMC HPC Interface

- VITA 57.1 Specifications compliant
- Single Module Width 69mm, Depth 76.5mm
- 4x MGT DP[3:0]_M2C, 4x MGT DP[3:0]_C2M for JESD204B/C interfaces up to 24.33Gbps
- 2x MGTCLK[1:0]_M2C
- LA Bus for LVDS and Single-Ended signals
- VADJ = 2.5V to 1.5V

Board Main ADI Components

- ADRV9026 : Integrated, Quad RF Transceiver
- AD9528 : JED204B Clock Generator with 14 LVDS/HSTL Outputs
- AD7291 : 8-Channel, I2C, 12-bit SAR ADC with Temperature Sensor

RF Performances

- RF coverage 75MHz to 6.0GHz
- Tx synthesis bandwidth to 450MHz
- Rx bandwidth to 200MHz

On-board VCXO Options

- 100.000MHz
- 122.880MHz
- 153.600MHz
- 156.250MHz

Front Panel I/O: 10x micro SSMC Connectors

- TX Transmitter Channel 1 Output
- TX Transmitter Channel 2 Output
- TX Transmitter Channel 3 Output
- TX Transmitter Channel 24Output
- RX Receiver Channel 1 Input
- RX Receiver Channel 2 Input
- RX Receiver Channel 3 Input
- RX Receiver Channel 4 Input
- Ext_Lo Input/Output
- External Reference Clock Input

Environnemental Specifications

- Commercial Ruggudized 0-50C
- Conduction Cooled -40C to 70C at Thermal Interface

Product Codification

The FMC-ZU3RF-B can be assembled with different versions. The cooling technique et ruggedization level are also available options. The following table shows the product coding for all these options.

FMC-ZU3RF-B– M 2 A – AS

	Tuning Frequency Range	
M	Middle	650MHz - 6GHz

	VCXO Frequency
1	100.000 MHz
2	122.880 MHz
3	153.600 MHz
4	156.250 MHz

	User Option
A	No Option

	Ruggedization Level	VITA 47
AS	Air Standard	EAC4
AR	Air Rugged	EAC6
CC	Conduction Cooled	ECC3
CR	Conduction Rugged	ECC4

Ordering Information

The following product references are offered by PanaTeQ as standard products. Other combinations of devices, speed grade, memory and cooling can be specially ordered. Please contact us for details

Reference	Tuning Range	VCXO	Front User SSMC	Ruggedization Level
FMC-ZU3RF-B-M1A-AS	650MHz - 6GHz	100.000MHz	REFCLKIN	Air Standard Cooled
FMC-ZU3RF-B-M1A-CC	650MHz - 6GHz	100.000MHz	REFCLKIN	Conduction Cooled
FMC-ZU3RF-B-M2A-AS	650MHz - 6GHz	122.880MHz	REFCLKIN	Air Standard Cooled
FMC-ZU3RF-B-M2A-CC	650MHz - 6GHz	122.880MHz	REFCLKIN	Conduction Cooled

Reference	SDR System Development
VPX3-ZU1B-SDR-DB	4U Desktop Chassis Air Cooled, VPX3-ZU1B, RTM-ZU1-A, FMC-ZU3RF-B, Linux BSP, Cables

PanaTeQ

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Available from: